

U.S. Department of Commerce, Patent and Trademark INFORMATION DISCLOSURE STATEMENT BY APPLICANT.		Atty. Docket No. SNDK.310US0	Application No. 10/600,259			
(Use several sheets if necessary)		Applicant(s) Jeffrey Lutze et al.				
		Filing Date 06/20/03	Group Unknown			
U.S. Patent Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
T	001 6,529,410	3/2003	Han et al.			
	002 6,295,227	9/2001	Sakui et al.			
	003 5,640,032	6/17/1997	Yugo Tomioka, Tokyo (JP)			
	004 5,070,032	12/3/1991	Yuan et al.			
	005 5,923,976	7/13/1999	Kim			
	006 6,297,097	10/2/2001	Jeong			
	007 5,981,335	11/9/1999	Chi			
✓	008 5,343,063	8/30/1994	Yuan et al.			
U.S. Published Patent Application Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
T	009 U.S. 2002/0093073	7/18/2002	Mori et al.			
T	010 U.S. 2004/0070021	4/15/2004	Yuan, Jack H.			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
T	011	International Search Report, PCT/US03/32119 filed 08/10/2003				
	012	U.S. Patent Application No. 09/667,344, Yuan et al. 9/22/2000.				
	013.	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.				
	014.	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.				
✓	015	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.				
Examiner	<i>Wade</i>	Date Considered 8/9/2004				
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>						

U.S. Department of Commerce, Patent and Trademark		Atty. Docket No.	Application No.			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		SNDK.310US0	10/600,259			
(Use several sheets if necessary)		Applicant(s)				
		Jeffrey Lutze et al.				
		Filing Date	Group			
		06/20/03	Unknown			
U.S. Patent Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
U.S. Published Patent Application Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
T	016	Hori et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," IEDM 92, April 1992, pp. 469-472.				
	017	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.				
	018	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.				
	019	Eitan et al., "NRROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.				
✓	020	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.				
Examiner <i>Thawle</i>	Date Considered 8/25/04					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>						